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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,319	02/09/2005	Farid N. Najm	361007-000043	6437

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EXAMINER	
KING, DOUGLAS	
ART UNIT	PAPER NUMBER
2824	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/524,319	NAJM ET AL.	
	Examiner	Art Unit	
	Douglas King	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-5 and 9-13* is/are allowed.

6)☒ Claim(s) *2,7,8 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Amendment

Acknowledgment is made of applicant's Amendment, filed 8 February 2007. The changes and remarks therein have been considered.

Claims 1, 6 and 14 have been canceled and claims 18, 19 and 20 have been added by Amendment. Therefore, claims 2-5, 7-13, and 15-20 are pending in the application.

Drawings

1. The drawings were received on 8 February 2007. These drawings are acceptable.

Specification

2. Claims 20 and 15 are objected to because of the following informalities:

   a. Claim 20, lines 6 and 10 recite "the word line" for which no antecedent basis exist. To expedite examination, the examiner has applied art consistent with --a word line--

   b. Claim 20 and claim 15 recite "the pull-down transistor" and "the pass transistor" which lack proper antecedent basis. The examiner believes these limitations to be referring to the "drive transistor" and the "access transistor" respectively, which appear earlier in independent claim 20 since there is no

support for an additional pass or pull-down transistor. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 2, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomotani (U.S. Patent 6,188,628).

Regarding independent claim 18, Tomotani discloses (Figure 2) an asymmetric SRAM cell for storing a binary variable, the asymmetric SRAM cell having reduced leakage power with respect to a comparable symmetric SRAM cell when the asymmetric SRAM cell stores a binary variable representing a predetermined binary value (see column 7, starting line 57, "for suppressing off leakage current), the asymmetric SRAM cell comprising : a first circuit comprising a plurality of transistors including a load transistor (See Figure 2, 20) , a drive transistor (22), and an access transistor (24), wherein the plurality of transistors within the first circuit include at least one first type of transistor (24, low Vt, see column 7, starting line 60) and at least one second type of transistor that is weaker than the first type of transistor (20 and 22 have high Vt, and therefore "weaker"); and a second circuit comprising a plurality of transistors including a load transistor (21), a drive transistor (23), and an access

transistor (25), wherein the plurality of transistors within the second circuit include at least one first type of transistor (25, low Vt) and at least one second type of transistor that is weaker than the first type of transistor (21 and 23 have high Vt, and therefore "weaker"), wherein the first and second circuits are operably coupled and configured as an asymmetric SRAM cell such that the configuration of the asymmetric SRAM cell achieves reduced leakage power with respect to a symmetric SRAM cell having the first type of transistor only (again see column 7, starting line 57, "for suppressing off leakage current").

Regarding dependent claim 2, Tomotani discloses the asymmetric SRAM cell of claim 18, wherein at least one of the second type of transistor is a transistor having a higher voltage threshold voltage as compared to the voltage threshold of the first type of transistor (see rejection to claim 18 above).

Regarding independent claim 19, Tomotani discloses an SRAM device (see Figure 2) comprising: an array of SRAM cells wherein each SRAM cell stores a binary variable representing a predetermined binary value, and each SRAM cell is an asymmetric SRAM cell having reduced leakage power with respect to a comparable symmetric SRAM cell (see column 7, starting line 57, "for suppressing off leakage current), each asymmetric SRAM cell comprising: a first circuit comprising a plurality of transistors including a load transistor (See Figure 2, 20), a drive transistor (22), and an access transistor (24), wherein the plurality of transistors within the first circuit include at least one first type of transistor (24, low Vt, see column 7, starting line 60) and at least one second type of transistor that is weaker than the first type of transistor (20 and 22

have high Vt, and therefore "weaker"); and a second circuit comprising a plurality of transistors including a load transistor (21), a drive transistor (23), and an access transistor (25), wherein the plurality of transistors within the second circuit include at least one first type of transistor (25, low Vt) and at least one second type of transistor that is weaker than the first type of transistor (21 and 23 have high Vt, and therefore "weaker"), wherein the first and second circuits are operably coupled and configured as an asymmetric SRAM cell such that the configuration of the asymmetric SRAM cell achieves reduced leakage power with respect to a symmetric SRAM cell having the first type of transistor only (again see column 7, starting line 57, "for suppressing off leakage current").

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 15, 16 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi (USPGPUB 2003/0002328).

Regarding independent claim 20, Yamauchi discloses an asymmetric static random access memory (SRAM) cell (see Figure 1) operable with a supply voltage to

store a one or a zero, the asymmetric SRAM cell further comprising: a first circuit comprising a plurality of transistors including a load transistor (MP1), a drive transistor (MN1), and an access transistor (MN3), wherein the load transistor and the drive transistor are coupled to form an inverter (MN1 and MP1 form an inverter) and the access transistor connects an output of the inverter to a bit line (RBL) when a word line (WLR) is held high (via MN3); a second circuit comprising a plurality of transistors including a load transistor (MP0), a drive transistor (MN0), and an access transistor (MN2), wherein the load transistor and the drive transistor are coupled to form an inverter (MP0 and MN0 form an inverter) and the access transistor connects an output of the inverter to a bit line (WBL) when a word line (WLWT) is held high (via MN3), wherein the first and second circuits are coupled to each other by connecting an input and an output of the inverter of the first circuit with those of the inverter of the second circuit in a cross-coupled manner (outputs and inputs of the two inverters are "cross coupled", see Figure 1); and a pass transistor (see objection above, MN3) connected to a gate of the pull-down transistor (MN0) so that a voltage across the gate is reduced relative to the supply voltage, thereby reducing leakage through the gate when the asymmetric SRAM cell is storing a zero (see paragraph 0028, "leak current...reduced to half")

Regarding dependent claim 15, Yamauchi discloses the asymmetric SRAM cell of claim 14 wherein a voltage at a gate of the pass transistor is reduced relative to the supply voltage to further reduce leakage through the gate of the pull-down transistor (see paragraph 0028)

Regarding dependent claim 16, Yamauchi discloses the asymmetric SRAM cell of claim 14, wherein the first and second inverters comprise a plurality of transistors further comprising at least one first type of transistor (Figures 1 and 2, transistor MN1) and at least one second type of transistor (Figures 1 and 2, transistor MN0) that is weaker than the first type of transistor (Figure 2, second transistor MN0 has higher threshold voltage and smaller gate (channel) width than first transistor MN1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomotani (U.S. Patent 6,188,628) in view of Meyer (US Patent No. 6,425,056).

Regarding claims 7 and 8, Tomotani discloses the SRAM device of claim 19 but does not explicitly disclose that the asymmetric SRAM cell device comprise an SRAM device selected from the group consisting of a direct store SRAM device or a selectively inverted SRAM device as in claim 7. Further, Yamauchi does not disclose that the SRAM device comprises a cache memory selected from the group consisting of a direct store cache memory and a selectively inverted cache memory as in claim 8. However, Meyer teaches the direct store (called direct mapped by Meyer) cache memory may include any of a wide-variety of suitable high-speed memory devices, particularly SRAM memory (Meyer, column 4 lines 7-12, and column 2 lines 49-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the asymmetric SRAM array of Tomotani in the direct store cache as taught by Meyer, for the benefit of reducing current leakage (see Tomotani, column 7, lines60-65).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi (USPGPUB 2003/0002328) in view of Greenberg (US Patent No. 10524319).

Regarding dependent claim 17, Yamauchi discloses the asymmetric SRAM cell of claim 16 but does not disclose the connection to a plurality of like cells and a sense amplifier further comprising pairs of cross-coupled inverters and a plurality of sens-amplifier transistor forming a dummy column of cells. However, the connections to pluralities of similar cells, the use of dummy or redundant columns, and the connection to sense amplifiers is common and well known in the art. For example, Greenberg

discloses a memory with cross-coupled inverter type sense amplifier and dummy memory cells connected therewith (see Figures 1, 2, and 6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to connect the memory cells of Yamauchi to like memory cells and construct a dummy column of memory cells with a sense amplifier for the benefits known in the art (e.g. using the dummy column for voltage reference during a reading operation).

Response to Arguments

7. Applicant's arguments filed 8 February 2007 have been fully considered but they are not persuasive.

Regarding independent claim 20, Applicant principally argues that Yamauchi does not describe the concept of individually varying transistors within each unit structure. To support this Applicant points to the multiple embodiments in the specification and Figures 3-12. The claimed structure has been addressed in the rejections above and although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

8. Applicant's arguments with respect to independent claims 18 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kuwazawa (USPGPUB 2003/0119265) discloses SRAM with "weaker" access transistors (see paragraph 0028).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas King whose telephone number is (571) 272-2311. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSK

ANH PHUNG
PRIMARY EXAMINER